stacked parallel to a substrate described in mode (1) is characterized by comprising steps of filling insulating films between rows of the stacked AAs, forming gaps as templates of gate electrodes in the insulating films, forming recesses in the AA sidewalls by using the insulating films as masks, and forming diodes by filling, in the recesses, semiconductor films having a conductivity type different from the AAs or by forming, on the surfaces of the recesses, semiconductor layers having a conductivity type different from the AAs by gas phase doping.

(Effect of Modes (17))

[0286] (a) It is possible to stack layers in a nonvolatile memory such as an RRAM or PRAM that senses the change in resistance.

[0287] (18) A semiconductor memory manufacturing method of forming electrodes of, e.g., an RRAM or PRAM in stripe-like active areas (AAs) stacked parallel to a substrate described in mode (1) is characterized by comprising steps of filling insulating films between rows of the stacked AAs, forming gaps as templates of gate electrodes in the insulating films, forming recessed diodes filled in the AA sidewalls by using the insulating films as masks, and filling electrode films in the recesses.

[0288] (19) A semiconductor memory manufacturing method of forming an RRAM described in mode (18) is characterized by comprising steps of filling first electrode films in recessed diodes filled in the sidewalls of stacked AAs, and forming memory dielectric films and second electrode films between rows of the AAs.

(Effects of Modes (17)-(19))

[0289] (a) It is possible to stack layers in a nonvolatile memory such as an RRAM or PRAM that senses the change in resistance.

[0290] (b) It is unnecessary to process the memory layer (a chalcogenide film that largely changes the resistance (normally, increases the resistance by thousand times) when heated in the case of a PRAM, and a metal oxide film such as TiO_2, HfO_2, ZrO_2, or nickel oxide in the case of an RRAM). This makes RIE processing of any new material unnecessary.

[0291] As described above, the embodiments of the present invention can provide a semiconductor memory having a structure in which memory layers can be stacked without largely increasing the number of process steps, and provide a method of manufacturing the semiconductor memory. In addition, the semiconductor memories disclosed in the embodiments make it possible to continuously increase the degree of integration of semiconductor memories, particularly, flash memories in the future. Accordingly, the range of applications of flash memories presumably further extends in the future.

[0292] Additional advantages and modifications will readily occur to those skilled in the art. Therefore, the invention in its broader modes is not limited to the specific details and representative embodiments shown and described herein. Accordingly, various modifications may be made without departing from the spirit or scope of the general inventive concept as defined by the appended claims and their equivalents.

1.-**20**. (canceled)

21. A semiconductor memory device comprising:

a semiconductor substrate including a first part having a first upper surface;

a plurality of first layers arranged along a first direction perpendicular to the first upper surface above the first upper surface and extending in a second direction parallel to the first upper surface, the plurality of first layers including first semiconductor layers stacked along the first direction;

a plurality of second layers arranged along the first direction above the first upper surface and extending in the second direction, the plurality of second layers being adjacent to the plurality of first layers in a third direction parallel to the first upper surface, the third direction intersecting the second direction, the plurality of second layers including second semiconductor layers stacked along the first direction;

a conductive layer disposed on the plurality of first layers and the plurality of second layers and covering the plurality of first layers and the plurality of second layers;

first memory portions disposed, in the third direction, between the conductive layer and first side surfaces of the first semiconductor layers, the first side surfaces being perpendicular to the first upper surface;

second memory portions disposed, in the third direction, between the conductive layer and second side surfaces of the second semiconductor layers, the second side surfaces being perpendicular to the first upper surface; and

a first selection transistor disposed on one of the first semiconductor layers.

22. The device according to claim **21**, further comprising:

a first contact portion electrically connected to a first end portion of the one of the first semiconductor layers in the second direction,

wherein the first contact portion is disposed between the first selection transistor and the first end portion.

23. The device according to claim **22**, further comprising:

a second selection transistor disposed on the other of the first semiconductor layers, the other of the first semiconductor layers arranged below the one of the first semiconductor layers in the first direction; and

a second contact portion electrically connected to a second end portion of the other of the first semiconductor layers in the second direction,

wherein the second contact portion is disposed between the second selection transistor and the second end portion, and

a first distance between the second contact portion and the second selection transistor in the second direction is shorter than a second distance between the second contact portion and the first selection transistor in the second direction.

24. The device according to claim **23**, wherein

a first length of the other of the first semiconductor layers in the second direction is longer than a second length of the one of the first semiconductor layers in the second direction.

25. The device according to claim **22**, further comprising:

a second contact portion electrically connected to second end portions of the first semiconductor layers in the second direction,